

Application No. 09/252,551

IN THE CLAIMS

Please amend Claims 134, and 142-144 as set forth below in reissue amendment format:

105  
1 134. (Amended) A bidirectional data communication system  
2 according to claim 104, wherein the first timing loop includes a  
3 high gain error generator, a loop filter, and an oscillator  
4 circuit, the high gain error generator responsive to characteristic  
5 values of the timing signals, and wherein the second timing loop  
6 includes a low gain error generator, a loop filter, and an  
7 oscillator circuit, the high gain error generator responsive to  
8 characteristic values of the data signals.

108  
1 142. (Amended) A bidirectional data communication system  
2 according to claim 107, the receiver block further comprising  
3 timing recovery circuitry coupled to receive the digital signal  
4 from the analog to digital converter and extract timing information  
5 therefrom, the analog to digital converter operatively responsive  
6 to said timing information and performing digital conversions at a  
7 rate defined thereby.

109  
1 143. (Amended) A bidirectional data communication system  
2 according to claim 108, wherein the timing recovery circuitry  
3 comprises a first timing loop having a high gain stage and a second  
4 timing loop having a low gain stage, the first timing loop locking  
5 the analog to digital converter in phase with the preamble portion  
6 the second timing loop locking the analog to digital converter in  
7 phase with the data containing portion.

110  
1 144. (Amended) A bidirectional data communication system  
2 according to claim 109, wherein the first timing loop includes a